A NEW TESTING SET-UP FOR INTEGRATED POWER METER

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Abstract – *The test set-up for Power meter IC is considered in this paper. Integrated Power Meter is a SoC dedicated not only for energy measurement but for measuring of many important power line signal parameters including RMS current and voltage, active, reactive and apparent power, power factor and frequency. The presented test set-up is considered here from the hardware and software point of view. Its main advantages are low cost, high efficiency and eas-to-use graphical user interface.*

1. INTRODUCTION

The successful implementation of integrated systems on chip depends not only on inventing and implementing the new circuits but also on the development of appropriate environment for prototype testing. Every new chip needs a test set-up capable to test its input and output interconnections, and to check the complete chip functionality. To fulfill all specified requirements, the set-up needs particular hardware and software.

This paper presents one application specific test set-up solution dedicated to the Integrated power-meter IC.

The paper is organized as follows. The second part gives a short description of functions and blocks built in the Integrated power-meter chip. The third section gives general description of the test set-up. The fourth section explains the hardware of the test set-up while the fifth chapter describes testing procedures. A short overview of the protocol that enabled efficient data acquisition will be given as well. The last chapter presents advantages of the used test set-up.

2. OVERVIEW OF INTEGRATED POWER METER

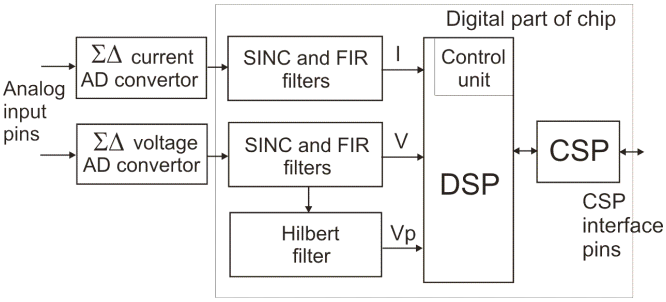

Figure 1. *Power meter System-on-Chip*

Integrated power-meter (IPM), which is implemented in 0.35μm CMOS standard cell technology, performs several functions: four quadrant power and energy measuring, instantaneous and RMS current and voltage levels, power factor and frequency.

Figure 1 shows structure of IPM. The analog front-end consists of two Sigma-Delta AD converters (for current and voltage channels) and Band-Gap voltage reference [1]. The digital part includes five digital filters (two Sinc, two FIR and one Hilbert transformer filter), Digital signal processing (DSP) block and Serial Communication Port unit (CSP).

The digital filters decimate oversampled signals coming from ADC output. Different resolution needed for current and voltage channel requires two separate decimation channels each with total decimation factor of 128. Both decimation channels consist of two Sinc filters and two FIR filters. The detailed description of filters can be found in [2].

Digital filters produce 24-bit signed two's complement digital samples of current I, voltage V and phase shifted voltage Vp that enter the DSP part (Fig. 1). Data rate of these voltage and current samples is 4096 Hz.

DSP block (Fig. 1) operates on 4.194 MHz clock frequency and calculates current and voltage RMS values, apparent, active and reactive power, power factor, frequency, reactive and active energy. Detailed description of DSP performances and realization can be found in [3], [4], [5].

Communication between IC core and external micro-processor is performed through the Communication Serial Port block (CSP in Fig. 1) that allows the user to calibrate components of IPM and read the measured results. Bidirectional pins SDA and SCL are used as communication interface. One additional pin - CSN enables the CSP block. More details about CSP realization can be found in [6].

IPM operates in four modes selectable by pins MODE1 and MODE0 [7]. Namely these are normal operating mode (NOM), testing mode (TM), initialization (INI) and reset mode (RST).

3. TEST SET-UP OVERVIEW

The simplified schematic of the test set-up is given in Fig. 2. The set-up consists of NI-6251 PCI DAQ card, the referent power-meter unit and specially designed printed circuit board which comprises IPM as unit under test and testing procedures.

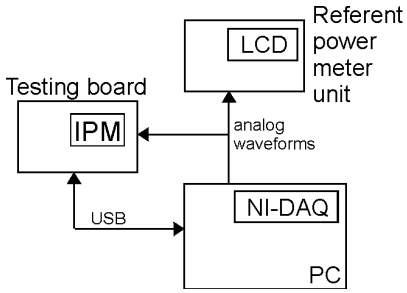

Figure 2. *Integrated power-meter set-up overview*

USB port connects the printed circuit board with the PC providing 5V power supply from PC to the board.

NI-DAQ card generates analog sinusoidal waveforms to stimulate current and voltage inputs of IPM. As IPM requires differential input signal, the both analog output of the DAQ card are used. These signals have maximal amplitude of 500mVpp. *LabView* software controls the card operation.

Analog stimuli are loaded simultaneously into the test board and the referent power meter unit (Fig.2).

The referent power meter unit (RPMU) is developed by our industrial partner. It is a modified standard power meter adapted for purpose of IPM calibration and testing. The signals from NI-DAQ are directly fed to the inputs of competitive integrated power-meter IC which is incorporated into this referent power meter unit. Therefore, current transformers and voltage divider circuits within power-meter are bypassed.

Specially designed printing circuit board (in further called simply the testing board) incorporates the IPM and circuitry needed to accept and store temporary data in the form suitable for transfer through USB port. The IPM receives analog waveforms from NI-DAQ and calculates power line parameters. The data are sent to the PC for further processing, recording and displaying. For this purpose, a specific software solution called *IPM Master* is specially developed using Visual C++ programming language. It is a graphical user interface that eases calibrating and testing procedure. It controls the operation mode of IPM and drives the data transfer to/from PC. The user can access to any of internal register in IPM and to read and/or write data as 24-bit word.

The following section describes the testing board in more details.

4. TESTING BOARD

Fig.3 presents the simplified schematic of the testing board. Except IPM that is unit under test, the main parts of the board are microcontroller PIC16F877 and RS232 to USB converter IC - FT232BM.

The board gets 5V power supply from PC via USB port. IPM operates at 3.3V and LT1085-3.3V is needed to provide the voltage reference. The rest of circuitry (including PIC microcontroller) operates at 5V. The analog inputs of IPM had to be isolated from USB port in order to provide safe operation during connecting testing board and external referent power meter unit. Therefore, isolated DC/DC converter IC - AM1S-0505 is used. Besides, serial communication lines (RX and TX lines) between PIC and FT232BM chip had to be isolated by using opto-couplers.

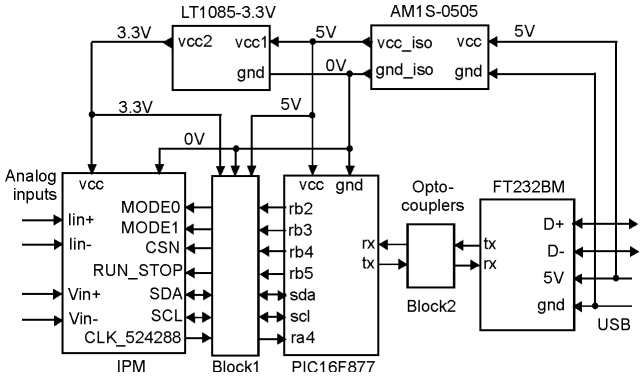

Figure 3: *Test set-up board for IPM testing*

Microcontroller controls the logical states on IPM input pins MODE1 and MODE0 that define the operating mode of IPM chip. Table I presents correspondence between chip operating mode and logical states on MODE1 and MODE0.

Microcontroller enables the communication with IPM over CSN pin.

Table I

IPM operating mode	MODE1	MODE0
Normal	0	0
Initialization	0	1
Testing	1	0
Reset	1	1

Since microcontroller and IPM operate at different power supply voltages, voltage level shifters are used for signal shifting from 3.3V to 5V and vice versa. They are incorporated within Block 1 in Fig. 2. Detailed internal structure of Block 1 is given in Fig. 4.

Inverters 74HCT04, open-drain inverter 74HC05 and pull-up resistors (Fig. 4) provides level shifting for signals MODE1, MODE0, RUN_STOP and CSN.

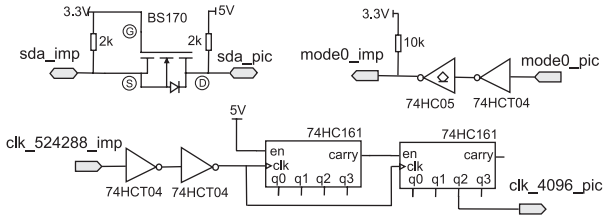

Figure 4: *The structure of Block 1 - voltage level shifters and clock divider circuit*

Bidirectional ports SDA and SCL on IPM and PIC microcontroller sides are interfaced through N-channel MOSFET transistors BS170 (Fig. 4).

The level shifting operation on SDA and SCL lines requires consideration of the following three states:

State 1. If neither IPM nor PIC microcontroller is pulling down the signal line, the signal line of IPM is pulled up to 3.3V. The gate and the source of the BS170 are both at 3.3V and V_{GS} is below the threshold voltage, hence the BS170 is not conducting. This allows that the line at PIC section is pulled up to 5V. Therefore, the lines of both sections are HIGH, but at a different voltage level.

State 2. If IPM chip pulls down the line to a LOW level, the source of the BS170 becomes also LOW, while the gate stay at 3.3V. The V_{GS} rises above the threshold and the BS170 starts conducting. Now, the line of the PIC microcontroller section is pulled down to a LOW level by the 3.3V device via the conducting BS170. So, the lines of both sections become LOW at the same voltage level.

State 3. PIC microcontroller pulls down the line to a LOW level. The drain-substrate diode of the BS170 conducts driving source to LOW. Simultaneously, V_{GS} exceeds the threshold, transistor BS170 conducts, driving the line of the IPM section further to LOW level defined by PIC. Therefore, the lines of both sections become LOW at the same voltage level.

The implementation of printed circuit board is given in Fig. 5.

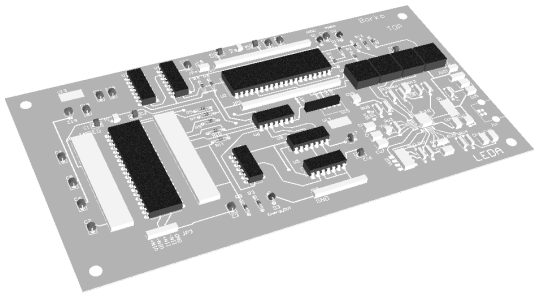

Figure 5: *Implemented printing circuit board*

5. *IPM MASTER* APPLICATION

Fig. 6 presents the main window of *IPM Master* GUI. It displays the following power-line parameters: measured RMS values for current (Irms) and voltage (Vrms), active (P), reactive (Q) and apparent (S) power, power factor (cos(fi)) , frequency (Freq), spent or generated energy value for active and reactive power (Pos. and Neg. Active and Reactive Energy). Each value is given in both formats: as hexadecimal number (representing the content of the appropriate register of IPM) and in physical units.

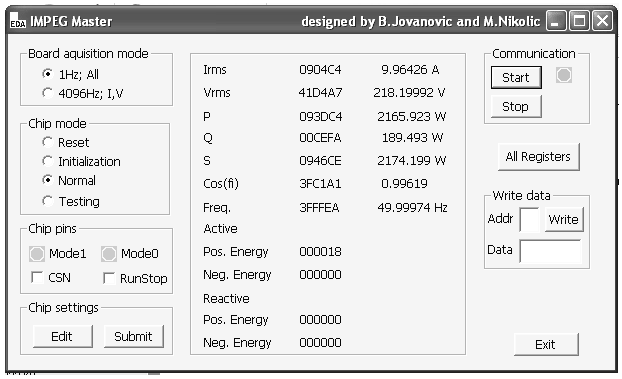

Figure 6: *The main window of IPM Master application*

IPM Master provides two different acquisition modes that control the PIC operation (group box Board acquisition mode shown in Fig. 6). In the first acquisition mode, PIC periodically collects contents from all 64 registers of IPM, while during the second mode, PIC only collects the data from registers for instantaneous current and voltage values.

Since the DSP part of IPM periodically calculates power-line parameters after every second in normal operating mode, PIC controller have to read new data from all registers and send data to the USB port, after the time interval. Synchronization between PIC controller and IPM chip is achieved through a particular IPM output pin which gives clock frequency equal to 524288Hz. This clock frequency is used as input to the clock divider circuit that partially belongs to Block 1 (Fig. 4) and the other part is implemented in PIC controller software. Clock divider in Block1 is formed by two 4-bit counters 74HC161 with the total clock dividing factor of 128. Clock frequency equal to 4096Hz is then fed into the pin RA4 of PIC microcontroller. Timer 1 of the PIC is then used to generate clock frequency of 1Hz that triggers the program routine implemented in PIC program. In this program routine PIC reads all registers and sends data to the FT232 over its RS232 serial interface (pin TX of PIC16F877 shown in Fig. 3).

The second acquisition mode is used when one needs only the instantaneous waveform samples of current and voltage signals. This is useful for performance analysis of AD converters and digital filters incorporated within the chip.

Digital filters of IPM produce 24-bit signed two's complement digital samples of current I, voltage V that enters the DSP part of IPM (Fig. 1). Data rate of waveform samples is 4096Hz. Clock frequency of 4096Hz from the Block1 is fed into the pin RA4 of PIC microcontroller that directly triggers the program routine which reads registers for I and V are send the data over RS232 serial interface.

The chip operating mode can be chosen by selecting one of four radio buttons: Reset, Initialization, Normal and Testing in the group box called Chip mode (Fig. 6). When one radio button is selected, *IPM Master* sends the appropriate command to the PIC to set appropriate logical states to pins MODE0 and MODE1 (Table I). The user can enable serial communication block of IPM by checking the CSN check box (Fig. 6).

When Edit button in the Chip settings group box (Fig. 6) is pressed, new dialog window appears on the screen, *Chip initialization*.

This window is used for selection of calibration registers that can be modified during the initialization mode. Beside, registers content can be changed by entering the 6-digit hexadecimal number into appropriate edit fields. While initialization mode is selected, after pressing *Submit* button (Fig. 6), calibration registers of the IPM are modified with the values previously defined in *Chip initialization* dialog.

IPM Master offers to user a possibility to change the content of any IPM register anytime during the normal operating mode. The access needs address to be written into *Addr edit* field in form of 2-digit hexadecimal number and data to be written into *Data field* in form of 6-digit hexadecimal number. Pressing the *Write* button causes modification of the selected register content.

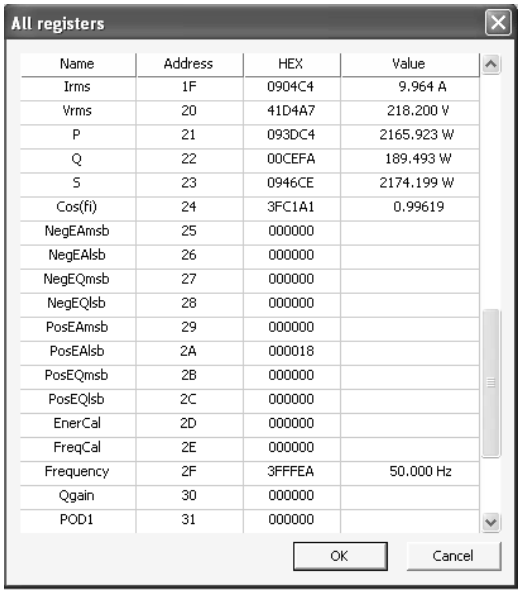

Figure 7: *Exploring content of all 64 registers of IPM chip*

Fig.7 one shows the application window that explores the content of all 64 registers of IPM chip. Each register is defined by the name, corresponding address value and content given in both formats: in a 6-digit hexadecimal number and in physical units.

Table II

REFERENT POWER METER			IPM			RELATIVE ERROR [%]		
V - REF	I - REF	P - REF	V - MER	I - MER	P - MER	V	I	P
392.98	97.045	38132.5	393.22	97.032	38210	-0.061	0.013	-0.203
357.85	88.378	31620	357.97	88.366	31697	-0.033	0.014	-0.243
314.88	77.758	24483	314.99	77.75	24537	-0.035	0.010	-0.221
287.79	71.044	20450	287.9	71.05	20494	-0.038	-0.01	-0.215
245.85	60.668	14925	245.98	60.72	14996	-0.053	-0.08	-0.476
200.71	49.56	9949	200.84	49.58	9980	-0.065	-0.04	-0.312
166.84	41.137	6873	166.95	41.21	6891	-0.066	-0.18	-0.262
134.67	33.203	4479	134.74	33.27	4489	-0.056	-0.20	-0.223
99.32	24.547	2436.3	99.37	24.53	2441	-0.056	0.069	-0.193
63.48	15.692	995	63.59	15.692	1010	-0.176	0	-1.508
47.32	11.701	553	47.417	11.704	554	-0.205	-0.03	-0.181
24.19	6.001	145.5	24.437	6.024	145.831	-1.021	-0.38	-0.227
12.28	3.024	37.5	12.52	3.07	36.846	-1.954	-1.52	1.744

6. CHIP VERIFICATION

Proper chip verification requires differential sinusoidal stimuli with maximum amplitude of 500 mVpp and maximum frequency of 200 Hz. This signal provides DAQ NI-PCI 6251 that has two analog outputs. The same signal stimulates tested IPM and a referent power meter unit. The obtained results are compared in PC. Calibration is the first step. It requires two measurements. One at low amplitude and the second with signal amplitude close to full range. Gain and offset is calculated for voltage, current and power. Calculated values are transferred to the proper IPM registers. After calibration measurements are performed for different amplitude of input stimuli. Table II presents results obtained during verification of one of prototyped IPMs. Suffix REF stands for referent values, while suffix MER stands for measured values of RMS voltage, RMS current and active power..

7. CONCLUSION

This paper presented test set-up for IPM consisting of hardware and software parts. This is cost effective solution for laboratory testing. The test set-up successfully fulfilled all imposed requirements. All measurements are done in real time. The chip under test is insulated from PC by opto-couplers and DC-DC converters.

ACKNOLADGE

The design described in this paper was founded by Serbian Ministry of Science and Environmental Protection within the project TR6108.

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Sadržaj – U ovom radu opisano je novo testno okruženje za testiranje integrsanog merača potrošnje električne energije. Opisani su hardverski i softverski delovi okruženja. Radi se o jeftinom uredjaju kojim se upravlja preko PC računara uz primenu softverske aplikacije specijalno razvijene za ove potrebe.

NOVO TESTNO OKRUŽENJE ZA TESTIRANJE INTEGRISANOG MERAČA POTROŠNJE ELEKTRIČNE ENERGIJE

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